National Semiconductor

MICROCIRCUIT DATA SHEET

MNLF411M-X REV 2A2

Original Creation Date: 06/21/95
Last Update Date: 07/16/02
Last Major Revision Date: 08/08/01

LOW OFFSET, LOW DRIFT JFET INPUT OPERATIONAL AMPLIFIER

General Description

This device is a low cost, high speed, JFET input operational amplifier with very low input offset voltage and guaranteed input offset voltage drift. It requires low supply current yet maintains a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF411 is pin compatible with the standard LM741 allowing designers to immediately upgrade the overall performance of existing designs.

This amplifier may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage and drift, low input bias current, high input impedance, high slew rate and wide bandwidth.

Industry Part Number

LF411

NS Part Numbers

LF411MH/883
LF411MWG-MLS
LF411MWG/883

Prime Die

LF411

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-833, Method 5005

Subgrp	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- Internally trimmed offset voltage. 0.5mV
- Input offset voltage drift. 10uV/ C
- Low input bias current. 50pA
- Low input noise current. 0.01pA/1/2 Hz
- Wide gain bandwidth. 3MHz
- High slew rate. 10V/uS
- Low supply current. 1.8mA
- High input impedance. 10[12]ohms
- Low total harmonic distortion Av=10, RL=10k, Vo=20 Vp-p, BW=20 Hz-20kHz. <0.02%
- Low 1/f noise corner. 50Hz
- Fast settling time to 0.01%. 2uS

(Absolute Maximum Ratings)

(Note 1)

Supply Voltage	±18V
Differential Input Voltage	±30V
Input Voltage Range (Note 4)	±15V
Output Short Circuit Duration	Continuous
Maximum Power Dissipation (Note 2, 3)	
H Package	670mW
WG Package	670mW
Tjmax	
H Package	150 C
WG Package	150 C
Thermal Resistance	
ThetaJA	
H Pkg (Still Air)	162 C/W
(500LF/Min Air Flow)	65 C/W
WG Pkg (Still Air)	170 C/W
(500LF/Min Air Flow)	120 C/W
ThetaJC	
H Pkg	20 C/W
WG Pkg	26 C/W
Operating Temperature Range	-55 C ≤ Ta ≤ +125 C
Storage Temperature Range	-65 C ≤ Ta ≤ 150C
Lead Temperature (Soldering, 10 seconds)	260 C
Package Weight (Typical)	
H Pkg	TBD
WG Pkg	220mg
ESD Tolerance (Note 5)	750V

Note 1: Absolute Maximum Ratings indicate limits beyond which damge to the device may occur. Operating Ratings indicate condition for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any temperature is Pdmax = (Tjmax - TA)/ThetaJA or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: Maximum Power Dissipation is defined by the package characteristics. Operating the part near the Maximum Power Dissipation may cause the part to operate outside garanteed limits.

Note 4: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 5: Human body model, 100pF discharged through 1.5K Ohms.

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vs = ±15V, Vcm = 0, Rs = 0

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vio	Input Offset Voltage	Rs = 10K Ohms			-2	2	mV	1
					-3.7	3.7	mV	2
					-3.3	3.3	mV	3
Iio	Input Offset Current				-0.1	0.1	nA	1
			3		-25	25	nA	2
Iib+	Input Bias Current				-0.2	0.2	nA	1
			3		-50	50	nA	2
Iib-	Input Bias Current				-0.2	0.2	nA	1
			3		-50	-50	nA	2
Vcm	Input Common Mode Voltage Range		1		±9		V	1, 2, 3
CMRR	Common Mode Rejection Ratio	Rs ≤ 10K Ohms, Vcm = ±9V			70		dB	1, 2, 3
+PSRR	Supply Voltage Rejection Ratio	+Vs = 6V, -Vs = -15V			70		dB	1, 2, 3
-PSRR	Supply Voltage Rejection Ratio	+Vs = 15V, -Vs = -6V			70		dB	1, 2, 3
Is	Supply Current					3.4	mA	1, 2, 3
-Ios	Output Short Circuit Current	+Vin = -11V, -Vin = 11V, Rs = 10K Ohms			13	50	mA	1
					6	60	mA	2, 3
+Ios	Output Short Circuit Current	+Vin = 11V, -Vin = -11V, Rs = 10K Ohms			-50	-13	mA	1
					-60	-6	mA	2, 3
+Vioadj	Input Offset Voltage Adjustment				8		mV	1
-Vioadj	Input Offset Voltage Adjustment					-8	mV	1
+Avs	Large Signal Voltage Gain	Vo = 0 to 10V, Rl = 2K Ohms	2		25		V/mV	4
			2		15		V/mV	5, 6
-Avs	Large Signal Voltage Gain	Vo = 0 to -10V, Rl = 2K Ohms	2		25		V/mV	4
			2		15		V/mV	5, 6
Vo+	Output Voltage Swing	Rl = 10K Ohms, +Vin = 11V, -Vin = -11V, Rs = 10K Ohms			12		V	4, 5, 6

Electrical Characteristics

DC PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vs = ±15V, Vcm = 0, Rs = 0

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vo-	Output Voltage Swing	Rl = 10K Ohms, +Vin = -11V, -Vin = 11V, Rs = 10K Ohms		`		-12	V	4, 5, 6

AC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vs = ±15V, Vcm = 0, Rs = 0

Sr+	Slew Rate	Vout = -5V to 5V			8		V/uS	7
Sr-	Slew Rate	Vout = 5V to -5V			8		V/uS	7
Gbw	Gain Bandwidth Product				2.7		MHz	7

DC PARAMETERS: DRIFT VALUES

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: +Vcc = ±15V, Vcm = 0V. "Delta calculations performed on JANS and QMLV devices at Group B Subgroup 5 ONLY"

Vio	Input Offset Voltage				-1	1	mV	1
+Iib	Input Bias Current				-0.1	0.1	nA	1
-Iib	Input Bias Current				-0.1	0.1	nA	1

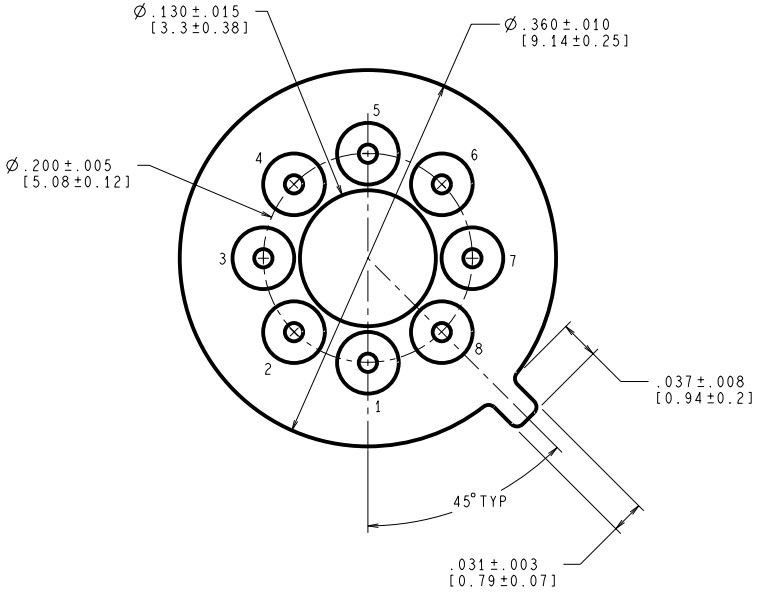
Note 1: Parameter guaranteed by CMRR test
Note 2: Datalog in K = V/mV.
Note 3: Rs = 10K Ohms at +125 C.

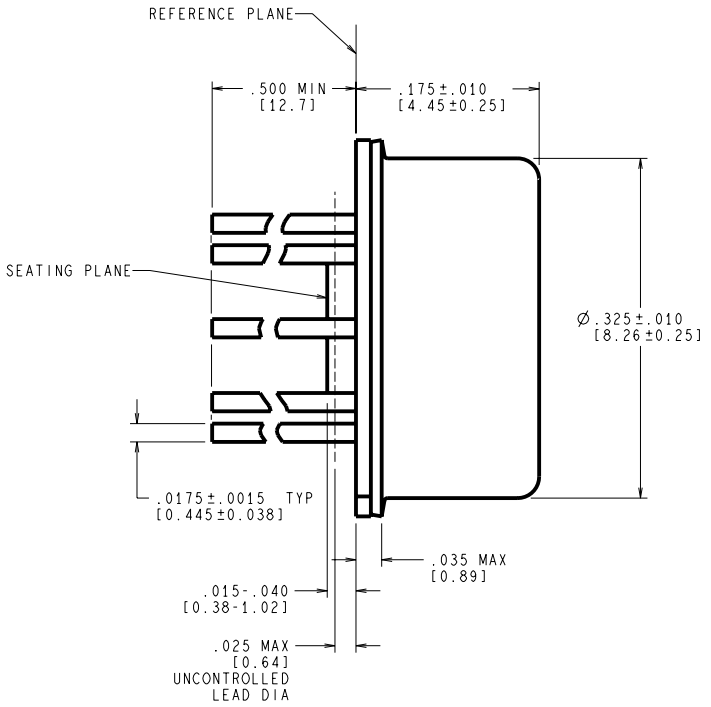
Graphics and Diagrams

GRAPHICS#	DESCRIPTION
05507HRA2	METAL CAN (H), TO-99, 8LD, .200 DIA P.C. (B/I CKT)
08337HRB3	CERAMIC SOIC (WG), 10 LEAD (B/I CKT)
09717HRB2	CERAMIC SOIC (WG), 10 LEAD (B/I CKT)
H08CRF	METAL CAN (H), TO-99, 8LD, .200 DIA P.C. (P/P DWG)
P000202A	METAL CAN (H), TO-99, 8LD, .200 DIA P.C. (PINOUT)
P000478A	CERAMIC SOIC (WG), 10 LEAD (PINOUT)
WG10ARC	CERAMIC SOIC (WG), 10 LEAD (P/P DWG)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
F	REVISE & REDRAW PER CURRENT STANDARD; UPDATE MIL/AERO STAMP & TITLE.	11002	06/22/95	MS/





CONTROLLING DIMENSION IS INCH
VALUES IN [] ARE MILLIMETERS

MIL-I-38535
CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEADS TO BE LOCATED WITHIN .007 IN/ 0.18 mm OF THEIR TRUE POSITIONS RELATIVE TO A MAXIMUM WIDTH TAB.
2. STANDARD METAL CAN TYPE: SOLID BASE WITH CERAMIC STANDOFF.
3. APPLIES TO MIL-AERO AND LINEAR PRODUCTS.
4. REFERENCE JEDEC REGISTRATION TO-99, JEDEC PUBLICATION No.95.

APPROVALS	DATE
DRAWN: MARTA SUCHY	06/22/95
DFTG. CHK.	
ENGR. CHK.	

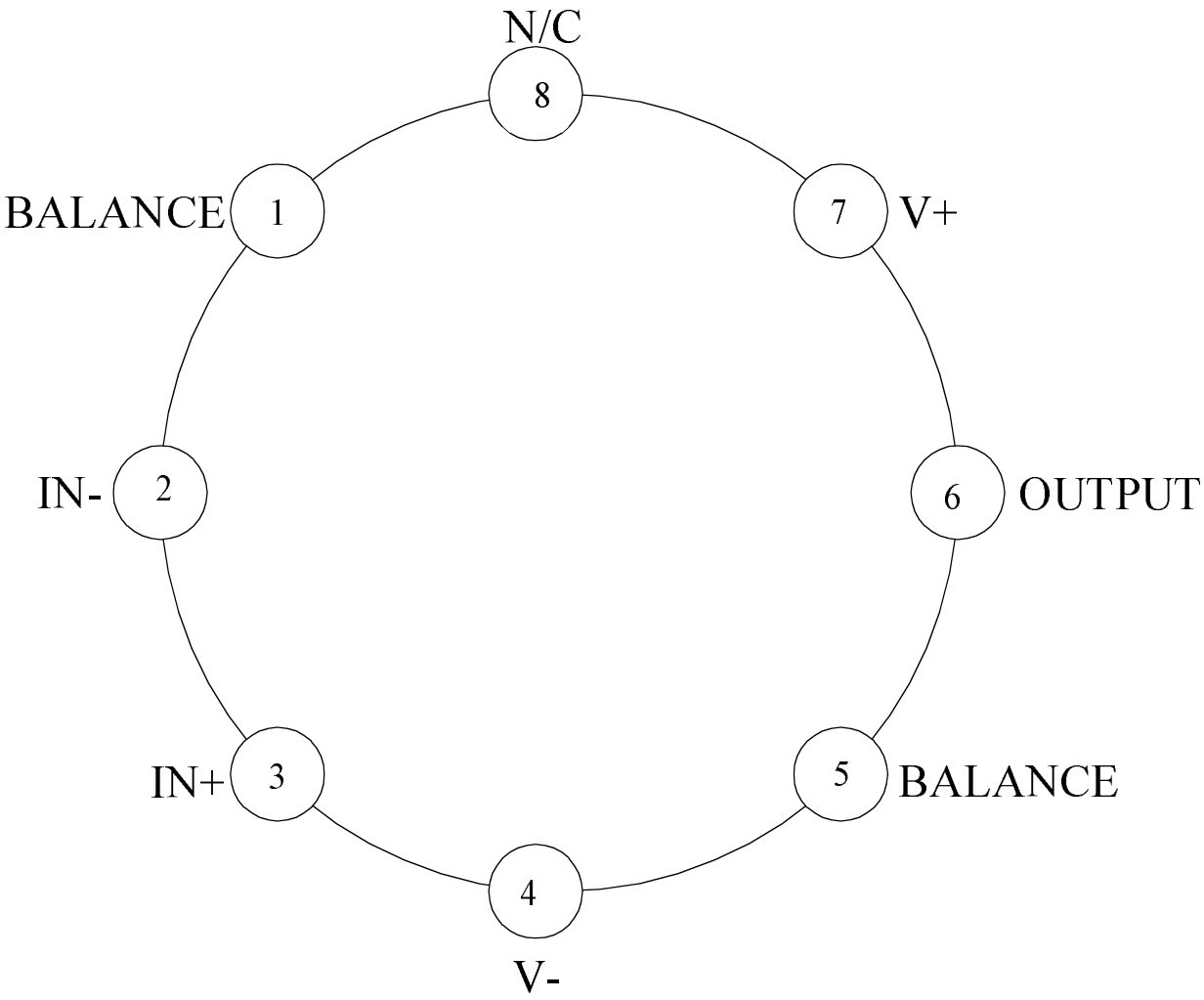
National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

METAL CAN, TO-99, 8 LEAD, .200 DIA P.C.

PROJECTION — INCH [MM]

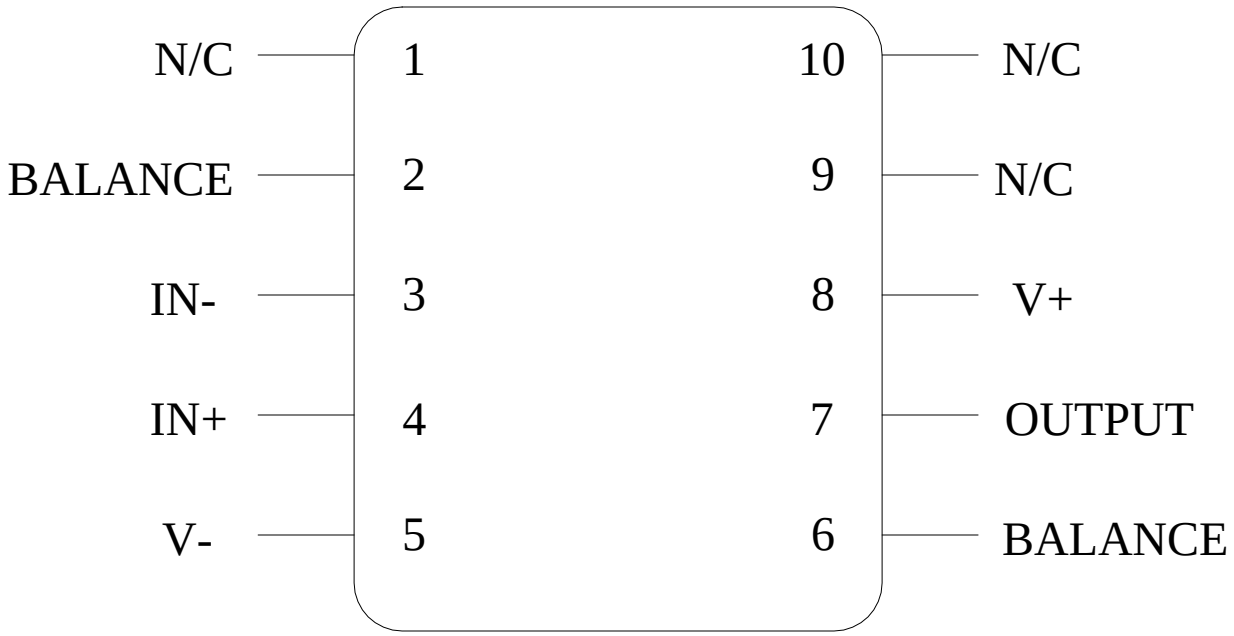
SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-H08C	F

DO NOT SCALE DRAWING — SHEET 1 of 1



LF411H
8 - PIN METAL CAN
CONNECTION DIAGRAM
TOP VIEW
P000202A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



LF411WG

10 - LEAD CERAMIC SOIC

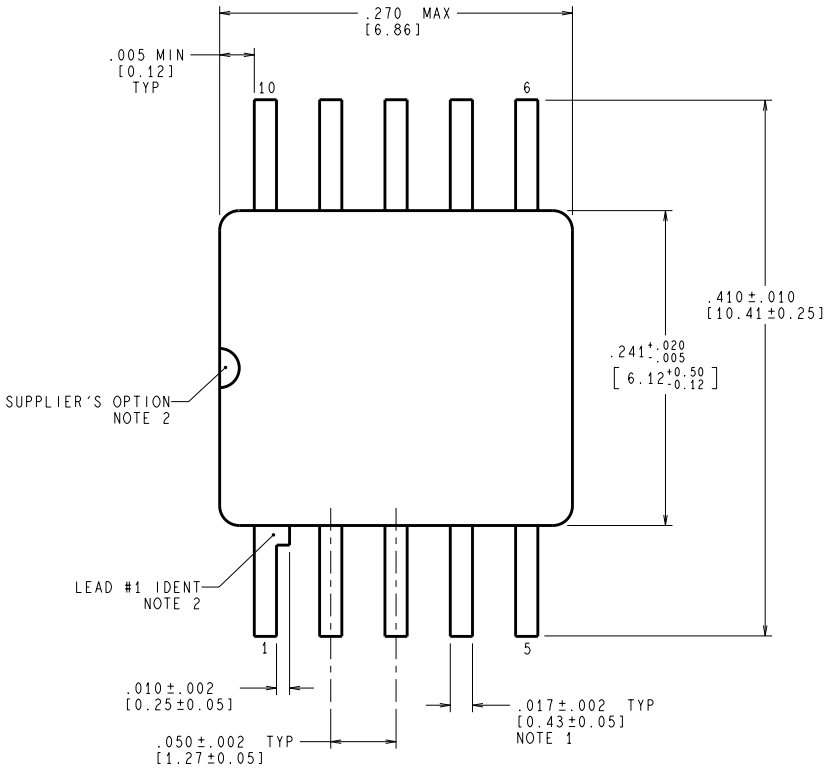
CONNECTION DIAGRAM

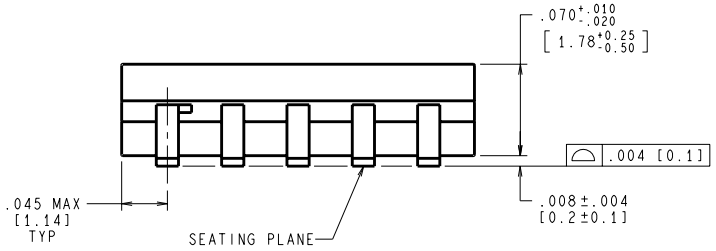
TOP VIEW

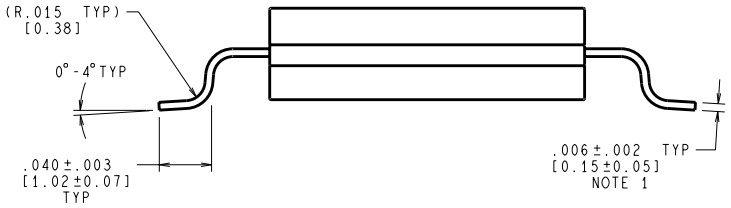
P000478A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	11374	02/29/1996	MS/KH
B	LD PITCH TOL WAS ±.005; CHANGE LD RADIUS TO REF DIM; REMOVE THE OTHER R.006±.002 DIM .040±.003 WAS .037±.003	11441	04/19/1996	MS/KH
C	R .015[0.38] WAS R .006[0.15]	11838	10/08/1997	TL/







NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-PRF-38535 TO A MINIMUM THICKNESS OF 200 MICROINCHES/ 5.08 MICROMETERS. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE. MAXIMUM LIMIT MAY BE INCREASED BY .003 IN/ 0.08mm AFTER LEAD FINISH APPLIED.
2. LEAD 1 IDENTIFICATION SHALL BE:
   a) A NOTCH OR OTHER MARK WITHIN THIS AREA
   b) A TAB ON LEAD 1, EITHER SIDE
3. NO JEDEC REGISTRATION AS OF FEBRUARY 1996.

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

MIL-PRF-38535
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN: MARTA SUCHY	02/29/96
DFTG. CHK.	
ENGR. CHK.	

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2900 Semiconductor dr, Santa Clara, CA 95052-8090

CERPACK, 10 LEAD, GULL WING

PROJECTION
INCH [MM]

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	(SC)MKT-WG10A	C

DO NOT SCALE DRAWING | SHEET 1 of 1

Revision History

Rev	ECN #	Rel Date	Originator	Changes
1A1	M0003840	07/16/02	Rose Malone	Update MDS: MNLF411M-X, Rev. 0BL to Fully Released MDS: MNLF411M-X, Rev. 1A1. Changed Electrical Section on the following parameters -Ios (Max Limits) Subgroup 1 from 45mA to 50mA, Subgroups 2, 3 from 45mA to 60mA. +Ios (Min Limits) Subgroup 1 from -45mA to -50mA, Subgroups 2, 3 from -45mA to -60mA. Due to Low yields.
2A2	M0004009	07/16/02	Rose Malone	Update MDS: MNLF411M-X, Rev. 1A1 to MNLF411M-X, Rev. 2A2. Added Drift Table to Electrical Section and Reference to WG Pkg.